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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/700,359      | 11/14/2000  | Roger Green Stewart  | RCA89038            | 4790             |

7590 03/26/2003

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EXAMINER

NELSON, ALECIA DIANE

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2675

DATE MAILED: 03/26/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

an

# Office Action Summary

Application No.

09/700,359

Applicant(s)

STEWART ET AL.

Examiner

Alecia D. Nelson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-6*** are rejected under 35 U.S.C. 102(b) as being anticipated by Shinya (U.S. Patent No. 5,170,158).

Shinya teaches an arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device (see abstract). The display device comprises a plurality of semiconductor switches, each having a first, second, and third terminal (see S/H), a control bus (see wires (SCK1-5)) coupled to a the terminals of each of the plurality of switches (right input terminal of S/H) for communicating corresponding signals, and a plurality of local buses (wires in groups of five from left input of the sample hold circuit to the DAC) that are separated from one another for communicating corresponding signals, a given local bus having a first bus section coupled to a second plurality of terminals associated with the given local bus (portion extending from DAC) and extending in a manner to cross over the control bus (over SCK1-5) and a second bus section extending from the first bust section and having conductors thereof coupled in a local, clustering bus arrangement (portion after crossing SCK1-5 ending in the left input of the sample hold circuits) to the second

terminals of switches associated with the given local bus of the plurality of switches, the associated switches having the third terminals thereof coupled to consecutively disposed column conductors (0<sub>0</sub>-0<sub>99</sub>), respectively of the array (see figure 18). With reference to **claim 2**, it is also taught a timing generator (14) providing switch control signals and DACs providing picture information signals to the S/H. Since each of the 20 outputs of the DACs is coupled to five sample hold circuits, a 1 of 5 demultiplexing is achieved under the control of the timing generator (14) (see column 9, line49-column 10, line19). With reference to **claim 3**, there is also disclosed that each of the sub groups is coupled to the same wire SCK of the timing generator (14) (see figure 18). With further reference to **claim 4**, Shinya teaches in figure 18 that the conductors of the second bus section of the given local bus are disposed in a vicinity of the switches associated with the given bus and remotely from switches associated with the other local buses of the plurality of local buses to provide bus separation for obtaining the local clustering bus arrangement (see figure 18). Referring to **claim 5**, it can be seen that the conductors of the first bus (SCK1-5) extend along the plurality of semiconductor switches. With reference to **claim 6**, it is further taught that the data line drivers are controlled by the wire OE from the timing generator.

3. **Claims 7-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (U.S. Patent No. 5,113,181).

With reference to the claims Inoue et al. teaches in figure 2 a n x m matrix wiring

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circuit connected to  $M$  signal lines ( $m < M$ ) for the  $N \times M$  active matrix (see col. 4, lines 2-8) for a display panel comprising a plurality of clusters of switches (6), each cluster having numbered switches 1 thru  $n$  arranged sequentially, and each switch (6) having respective input, output, and control terminals (see column 3, line 61) with control terminals of all switches in each cluster connected to a common control terminal (see col. 3, line 63-col. 4, line 12), and having respective output terminals coupled to successive data lines ( $S(1)$ - $S(n)$ ) on the display panel, a plurality of cluster of data buses, each cluster of data buses having numbered conductors 1 thru  $n$ , the numbered conductors of respective clusters of data buses being coupled to input terminals of corresponding numbered switches of a plurality of the clusters of switches, a control bus including a plurality of conductors, the control bus arranged to crossover the plurality of clusters of data buses (see column 3, lines 24-26, column 5, lines 30-37), and connections between one of the plurality of conductors ( $g(1)$ - $g(n)$ ) of the control bus and respective common control terminals of the cluster of switches (see figure 2).

### ***Response to Arguments***

4. Applicant's arguments filed 01/03/03 have been fully considered but they are not persuasive. With reference to **claims 1-6**, the applicant argues that Shinya neither discloses nor suggest a control buss connected to the first terminal of each of the plurality of switches, however this limitation is disclosed as recited above with reference to lines SCK1-5. Further, it is stated by the applicant that unlike the present invention, the plurality of local buses shown and described in Shinya cross each of the plurality of

control buses, however it is claimed that the first section of the first bus is to cross the control bus. The applicant continues by stating that unlike the present claimed invention, the first bus section of the plurality of local buses cross **only** the control bus, however this is not claimed. With reference to **claims 7-9**, the applicant again argues that Inoue et al. fails to disclose or suggest that the first bus section of the plurality of local buses cross over **only** the control bus. The claim recites that the control bus is arranged to cross the plurality of groups of data buses, therefore the applicant is arguing a limitation that is not claimed.

### ***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

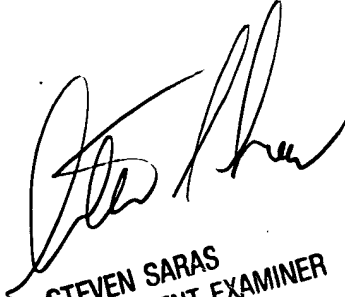
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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday 9:30-7:00, alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)305-6809 for regular communications and (703)305-6809 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9700.

adn/ADN  
March 20, 2003



STEVEN SARAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600